ABSTRACT OF THE DISCLOSURE

There is provided a phase locked state detecting apparatus for accurately detecting whether or not a phase locked state is canceled, the phase locked state detecting apparatus includes a comparator 17 for comparing a phase of a processing clock signal Smc generated by a phase locked loop for use in an information processing with a phase of a reference clock signal Src; an edge counter 18 for detecting a change of a frequency of the processing clock signal Smc; and a CPU 19 for judging to based on a phase comparison result whether or not the processing clock signal Smc is in the phase locked state with respect to the reference clock signal Src, and subsequently judging based on a detection result of the frequency change whether or not the phase locked state is canceled.